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High Accuracy Two-Step Flash ADC with Changeable Comparison Range Using Latch Based Comparator

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Abstract: Due to the technology development and decreasing supply voltages, undesirable effects on sensitive analog signals like noise, kickback are becoming more expressed. Mentioned issues are present in analog to digital converters (ADC) and design of high accuracy ADCs is becoming more complex. In this work, a circuit was proposed based on a latch comparator and comparison range shifter, which increased the accuracy of a two-step flash ADCs by excluding the chance of incorrect coarse conversion, when the input analog voltage is close to separating points of the comparison range of first stage of the ADC. The proposed circuit was constructed using an 16nm FinFET process, the simulations were done with HSpice simulator. The idea was to increase the accuracy of an already designed two-step flash ADC by adding the proposed circuit, which was done by shifting the comparison range during the coarse conversion, for the difference of input voltage and separating points not to be smaller than the offset of comparators used in ADC. It was established that the use of the proposed circuit increased the comparison time, as the sampled input analog voltage firstly should be compared with comparison range separating points, but on the other hand the ADC became more sensitive to its input change (up to 4mV offset) and was performing stable, excluding the chance of wrong coarse conversion. It has been shown that proposed architecture allows avoiding the use of low offset and high accuracy complex comparators in two-step flash ADCs, which greatly reduces the layout area.

Keywords: offset; latch; comparator; comparison range; sample and hold

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Высокоточный двухступенчатый АЦП с изменяемым диапазоном сравнения с использованием компаратора на основе защелки

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В связи с развитием технологий производства ИС и снижением напряжения питания в аналого-цифровых преобразователях (АЦП) наблюдаются нежелательные воздействия, например шума, других сигналов, на чувствительные аналоговые сигналы. Разработка высокоточных АЦП становится все более актуальной задачей. В работе рассмотрена схема с использованием компаратора на основе защелки и переключателя диапазона сравнения, повышающая точность двухступенчатых АЦП за счет исключения некорректного грубого преобразования, когда входное аналоговое напряжение близко к разделительным точкам диапазона сравнения первой ступени АЦП. Предлагаемая схема построена с использованием 16-нм FinFET-технологии, моделирование выполнено с помощью симулятора HSpice. Показано, что применение предложенной архитектуры позволяет избежать использования сложных компараторов с малым смещением и высокой точностью в двухступенчатых АЦП, в результате чего значительно уменьшается площадь компоновки. Рассмотренная схема для двухступенчатого АЦП выполнена путем сдвига диапазона сравнения во время грубого преобразования, для того чтобы разница входного напряжения и точки разделения не была меньше, чем смещение используемых в АЦП компараторов. Установлено, что использование предложенной схемы приводит к увеличению времени сравнения, так как дискретизированное входное аналоговое напряжение в первую очередь должно сравниваться с точками разделения диапазона сравнения, АЦП становится более точным (смещение до 4 мВ) и работает стабильно за счет исключения вероятности некорректного грубого преобразования.

Ключевые слова: смещение; защелка; компаратор; диапазон сравнения; выборка и хранение

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Introduction. Nowadays, technologies are developing and reaching down to 3 nm, supply voltages are becoming 0.75 V and lower. This means that any undesirable effects are becoming more expressed, such as leakage currents, noises on sensitive analog nets, kickback effects etc. [1–3]. Above mentioned effects are highly expressed in analog to digital converters (ADC) and digital to analog converters (DAC) [4, 5], because they are directly working with sensitive analog signals, especially in applications where high accuracy is required. That

is why it is becoming more important to develop methods that would help to increase accuracy of the circuits that are directly working with sensitive analog voltages.

Particularly, above mentioned effects affect the ADC performance. As known, the main operating block of the flash ADCs are comparators, as well as in two-step flash ADCs. To increase conversion accuracy, it is obvious that more accurate comparators should be used. That is to use operational amplifiers with small offset and high gain. Although to design an operational amplifier with better working parameters compared with a typical one with a conventional differential pair, it is needed larger layout area, complicated matching techniques and complex design methods. In two-step flash ADC the accuracy issue is becoming more fatal, because if the first stage ADCs' comparator will fail the comparison, in case when the ADC input voltage is closer to separating points, the output of the ADC will be unexpected and not even close to a correct code. The idea is to use an additional circuit to increase the accuracy of the ADC without using complicated comparator designs. In other words, circuit addition to already balanced and tested ADC reduces its chance of failing when the input voltage is close to first stage's separating points.

There are several methods of designing low offset comparators, namely: comparators where its inputs are reconfigured from the typical structure along with a use of restricted clock for the tail current [6]; latch type comparators with elimination of usage of preamplifier stages before latch stage which was used to overcome latch offset voltage [7]; using offset cancelation by storing it on the input capacitors of differential pair [8, 9] and interpolation [10, 11]. In this study, the idea is to increase the conversion accuracy of an already designed two-step flash ADC by adding a latch based comparator, instead of replacing all its comparators with more precise ones.

The main idea of the proposed architecture is to compare the input voltage with the first stage's separating points and, if the difference is close to comparator offset used in ADC, to shift the input range by some step, for the input to already be near to the middle of the separating points. Clearly, the comparison cannot be done with a low offset comparator, otherwise the whole approach would be useless, because we would be able to use that lower offset comparator directly inside the two-step ADC. The comparison would be done with a latch based comparator, described in [12].

Proposed circuit concept. High accuracy two-step flash ADC is presented, with adjustable comparison range, using a latch based comparator on the input (Fig.1). The main idea of the proposed circuit is to increase the accuracy of the two-step flash ADC when the input voltage is close to separating points of the conversion range, when coarse converting the most significant bits (MSB). In other words, when the input voltage and separating point difference is close to offset of the comparator used in MSBs converting part of the ADC, the chance of false coarse conversion lowers.

Sample and hold circuit is used to capture the analog signal and hold its value until the ADC will completely process the information. The analog signal after sample/hold block goes to latch based comparator, to be compared with separating points. That comparator's output signal is controlling the supply voltage shifter. It decides the comparison range for the whole two-step flash ADC, particularly for MSB coarse conversion. Supply voltage shifter generates the new supplies for the whole ADC as well as the control voltages for switches. The switches then are connecting the already defined voltages to higher and lower edges of the comparison range. In the proposed example the comparison range is shifting higher by ΔV amount. ΔV can be defined depending on the comparison range and the number of bits of MSB. For example, if we have a comparison range of 400 mV and 2-bit MSB converter, each section of the

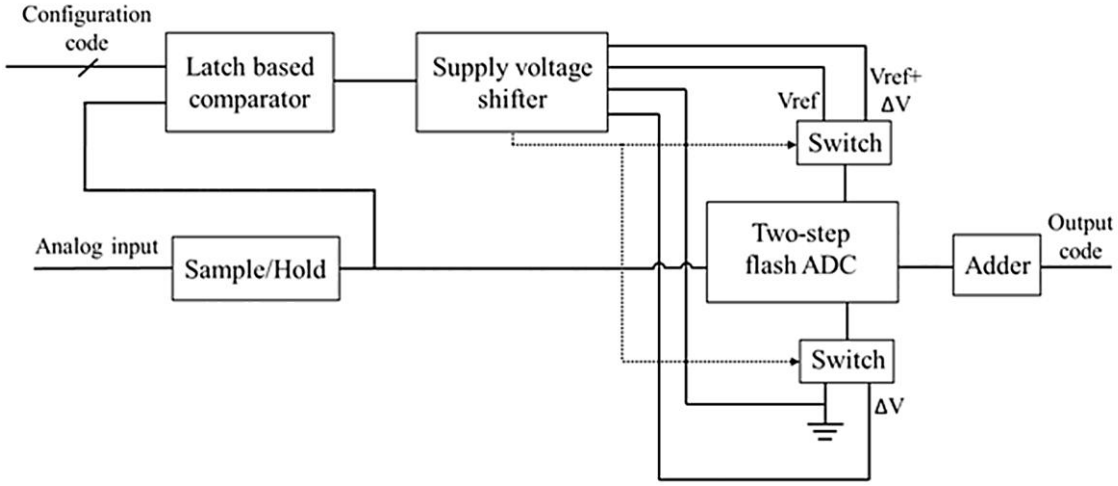


Fig.1. Block diagram of the proposed architecture

conversion range is equal to 100 mV and the separating points are 100 mV, 200 mV and 300 mV. In this case the ΔV can be set to 50 mV, for the input voltage to surely be in the middle of above mentioned sections after shifting. Then the two-step ADC will function as usual (detailed description is given in next sections), but with already shifted range. When the output code would be ready, the last thing to do is to sum the output code and the code corresponding to ΔV voltage. Note that the initial comparison with latch based comparator should be done only for inner separating points. For the higher and lower edges there is no reason for the comparison, because if the input would be close to Vref or ground, incorrect MSB conversion is not possible.

Higher accuracy for two-step flash ADC is achieved by lowering the possibility of a wrong coarse conversion, when the input voltage is close to separating points. It is done by some additional circuits, which are the latch based comparator, the circuit which shifts the comparison range and an adder to compensate the range shift.

Latch based comparator. To compare the sampled input a latch based comparator (Fig.2) is used [12]. The first stage converts the input voltage to current, that should charge the configurable capacitance. The main purpose of the first stage is to multiply a small input change to a much larger one on the output. Depending on the reference voltage, the input transistor is being kept in the linear operating region, to have the same change in drain current for a step change on gate, for different regions of the input swing. The reference voltage is defined by the total capacitance, which is set with the configuration code. Higher number of possible comparison reference voltages leads to more area of the configurable capacitance layout (more parallel capacitance fingers are needed). The switch control signals have a predefined timing, which is defined for some particular operation. During that time window the charges that managed to be accumulated on the capacitance will define the voltage going to

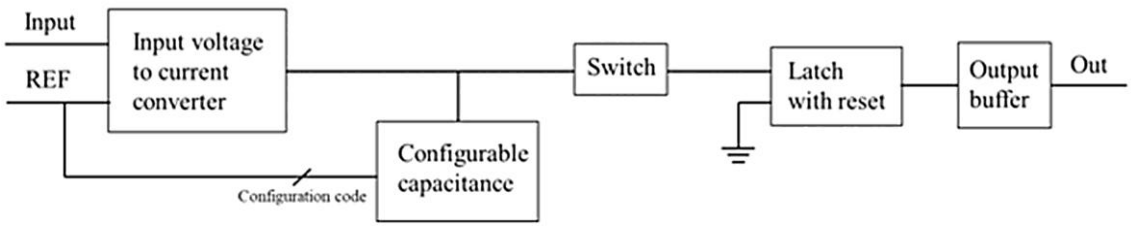


Fig.2. Block diagram of the latch based comparator

the latch input. The second input of the latch is connected to ground. By that the signals on the latch input are becoming like differential signals. And if the accumulated charge is enough, the latch will switch, which means that the difference between the input and reference voltages is bigger than the sensitivity margin. To exclude weak latch output switchings, a buffer is placed on the output to filter the latch output signal.

Implementation of the proposed method. Proposed circuit is implemented by integration of latch based comparator in two-step flash ADC circuit (Fig.3). The circuit consists of latch based comparator, the circuit which switches the comparison range, two-stage flash

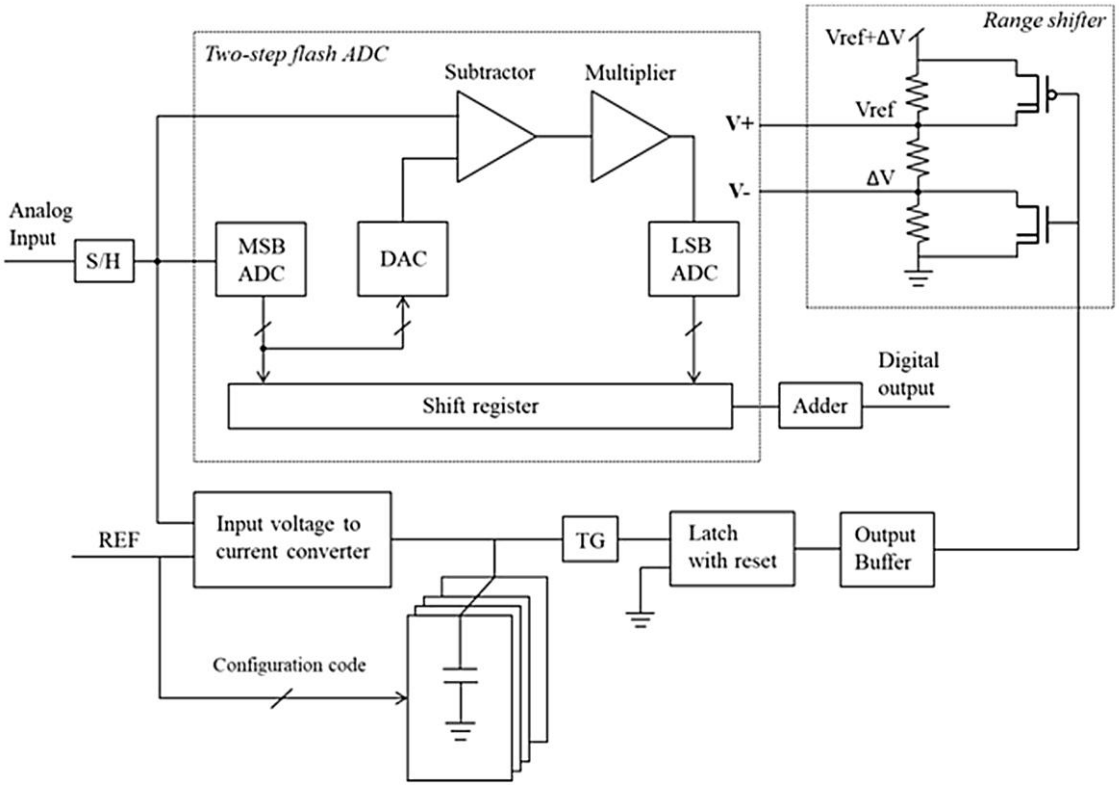


Fig.3. Implementation of the proposed architecture

ADC and an adder. Consider 2-bit MSB ADC. Number of least significant bits (LSB) ADC is not principal. In Fig.4 the comparison range and the separating points are shown. At the beginning of the conversion cycle the input analog voltage sampled with sample and hold circuit. As described in previous sections, the input voltage needs to be compared with V1, V2 and V3. At first the configuration code of the capacitor is selected to compare the input voltage with V1. After, the capacitor configuration code is changing to compare the input voltage with V2 and then with V3. In case if the analog voltage is neither close to V1 nor V2 nor V3, the two-step flash ADC functions as always, with comparison range from ground to Vref. If the input voltage is close to V1 or V2 or V3 (the difference is smaller than the initially defined value), the comparison range of the ADC should be

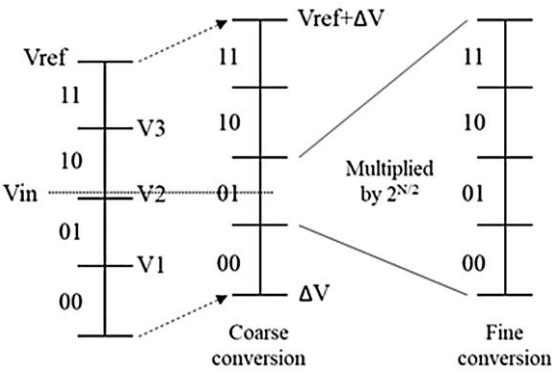


Fig.4. Conversion range shifting

shifted by some ΔV and become from ΔV to Vref + ΔV. V+ and V– depicted in the Fig.3 are the upper and lower edges of the comparison range. Range shifter circuit is used to shift the comparison range. The resistor sizes are set, for middle points to be equal to ΔV and Vref. A pair of NMOS and PMOS devices are used in range shifter. Depending on the voltage on the output of the latch based comparator, the V– and V+ would be connected respectively to 0 and Vref or ΔV and Vref + ΔV (one of the NMOS/PMOS pair would be shorted). ΔV can be defined by the following equation:

$$\Delta V = \frac{1}{2}\mathrm{Vref}\,\frac{1}{2^N} = \frac{\mathrm{Vref}}{2^{N+1}}. \quad (1)$$

By that after shifting the comparison range, the input voltage will be just about in the middle of separating points and the coarse conversion will be accurate, as depicted in Fig.4. And all the conversion up to the end would be done with shifted range. When the final code would be in the shift register, the code corresponding to ΔV would be added to get the ADC output by the adder.

Consider a case where the input voltage is close to V2 (Fig.4). In case of conventional ADC there is a probability that the MSB could be set to 01 and the whole conversion would be incorrect. In this case the comparison range is shifting and, as shown in Fig.4, the input voltage now is clearly in 01 range. After, the fine conversion would be performed and the code with shifted range would be defined. As the range is shifted up, and the obtained code is corresponding to a lower voltage than the input one, the adder would add the digital code of the ΔV to obtain the final code corresponding to input analog voltage.

Simulation results. The circuit of Fig.5 is implemented in the 16nm FinFET technology. All transistors in the circuit are regular voltage/threshold transistors. Simulations are done with HSpice simulator [13]. Supply voltage is 0.9 V, which is the nominal voltage for regular transistors.

The main components in Fig.5 are sample/hold block, latch based comparator, its output buffer, D flip-flop (DFF), range shifter and the flash ADC. Transient analysis is performed, as in the circuit non-parasitic capacitance is present. The input voltage sweeps from 600 mV to 610 mV with 1 mV step (delta on the waveforms). Capacitance value is set for the input voltage to be compared with 600 mV. The waveforms on Fig.6(*a*) show the latch performance. Latch buffered output (out 3), latch output (out 1), latch input (net 8), voltage on configurable capacitance (outin), transmission gate select signal (sel) and latch output enable signals (en_n) are shown. As can be seen from out 3 signals, the latch buffered output stops switching when input is 604 mV and lower. Detailed description of the latch-based comparator function can be found in [12].

The waveforms on Fig.6(*b*) show the range shifter performance. Latch buffered output (out3), clock signal of the DFF (clk), non-inversed output of the DFF (dff_out), lower (vl) and upper (vh) edges of the comparison range for the two-step flash ADC are shown. A two-step flash ADC is considered with a normal (non-shifted) comparison range from 400 mV to 800 mV and with 2-bit coarse conversion MSB ADC. The DFF is switching with a rise slope. Initially it is considered that the DFF output is logical 1 and the comparison range is from 400 mV to 800 mV. DFF is used to catch the latch buffered output value at the end of the comparison cycle. If the difference of the input and reference voltages is smaller than the sensitivity margin (4 mV), the configurable capacitance is not managing to accumulate enough energy to switch the latch, and the voltage on out 3 net remains 0. DFF catches the 0 on out 3 net, and its output is switching to 0. By (1) equation if the range is 400 mV and the MSB ADC is 2 bit, the range should be shifted by 50 mV. In range shifter block, the supplies

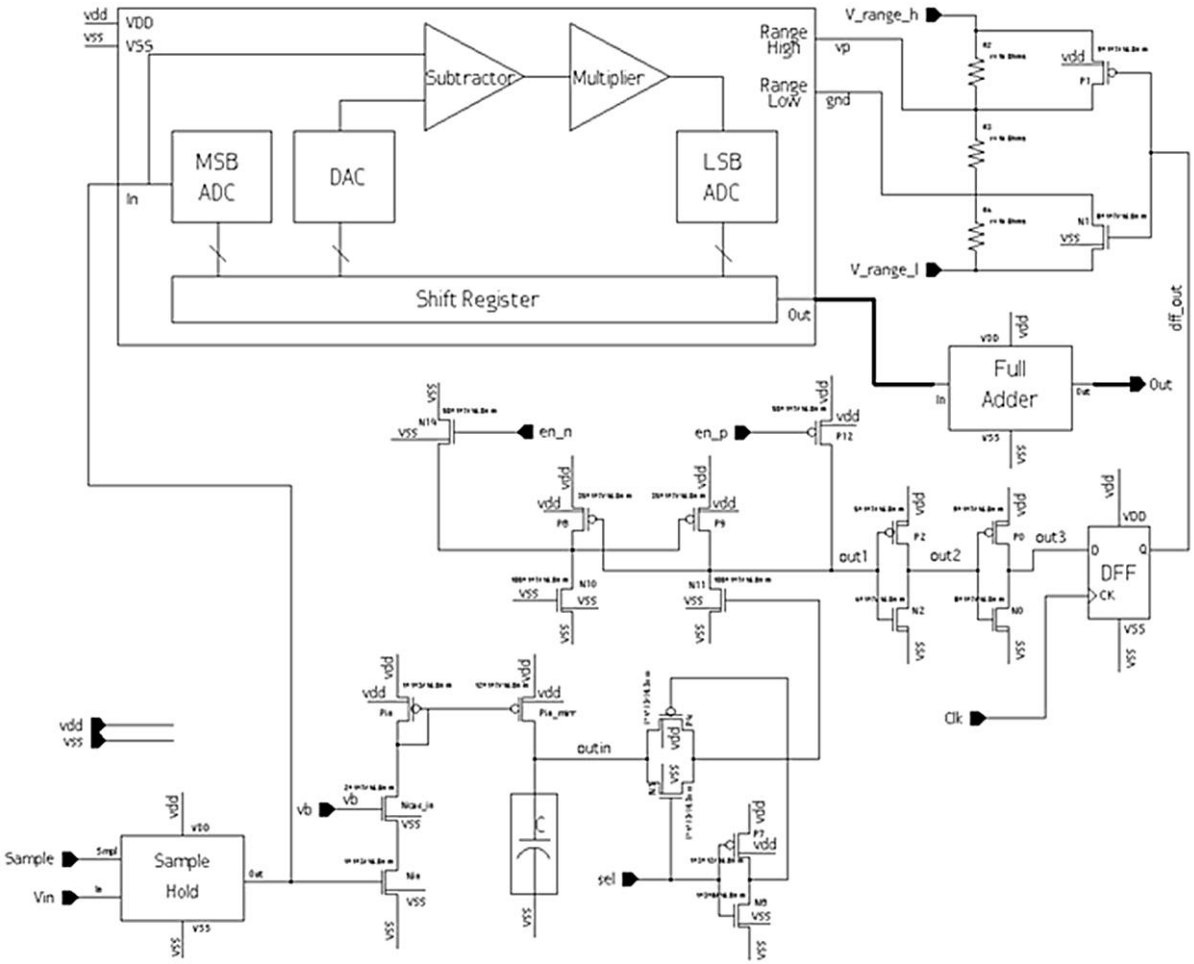
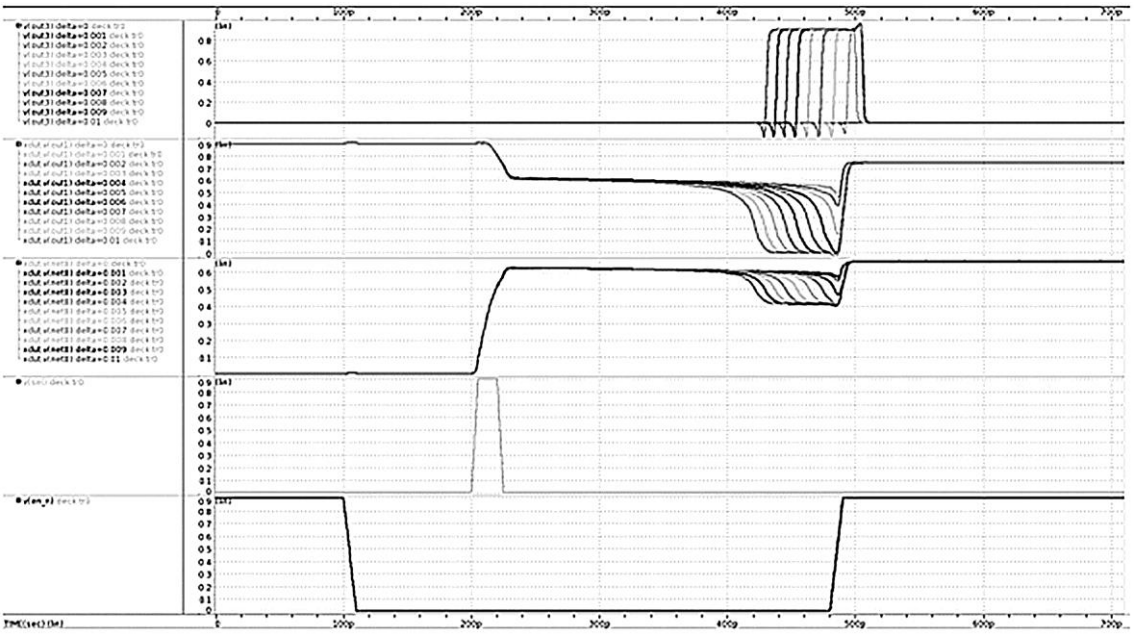


Fig.5. Schematic view of the proposed architecture

(V_range_h and V_range_l) are 850 mV and 400 mV respectively. The resistors sizes are chosen for the middle points to be 800 mV and 450 mV. When the DFF output is switching to 0, the PMOS is opening and NMOS is cutting off. By that on vh and vl nets the voltage is becoming 850 mV and 450 mV respectively. And if the input voltage would be close to 600 mV the adjacent separating points would be shifted to 550 mV and 650 mV. As can be seen from vl and vh waveforms, the range is shifting for delta values lower than 5 mV. For delta values 5 mV and above comparison range remains from 400 mV to 800 mV.

Same actions should be performed for every separating point (500 mV, 600 mV, 700 mV). And if the input voltage is close to either one of them, the range is shifting. When on the output of the two-step ADC the code would be available, the full adder would add the code corresponding to 50 mV and on its output the code corresponding to input voltage would be obtained.

In the simulated case a comparison cycle for one separating point lasts 400 pS. So, for 2-bit MSB ADC there are 3 separating points, and for this case comparison time will increase by 1.2 nS. For general case, the comparison duration increase would be $(2^N–1)\cdot 400$ pS, where N is the number of bits of MSB ADC. Area of the given circuit equals to around 53.6 μm^2 (excluding the full adder). Area is a strong function of the size of configurable capacitance, which means that the more combinations the configurable capacitance would have, the larger would be the circuit area.



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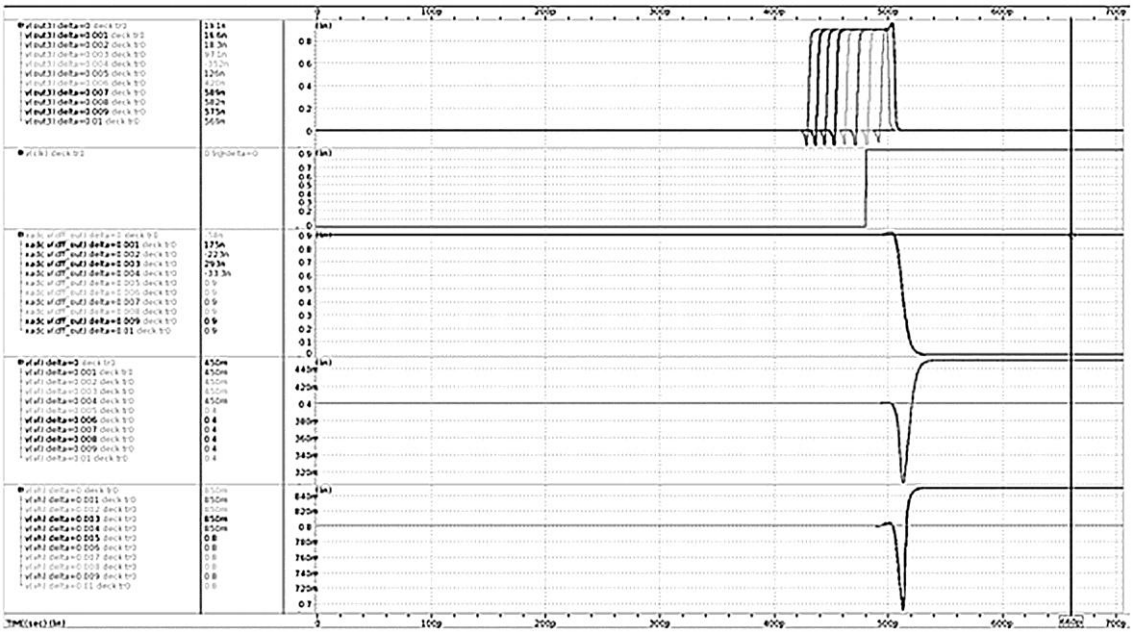

б

Fig.6. Latch based comparator performance (*a*) and range shifter performance (*b*)

Conclusion. A high accuracy two-step flash ADC with changeable input range has been presented, using a latch based comparator. To avoid designing low offset sensitive comparators, which will require complicated design and layout process and using them in ADCs will dramatically increase the ADC area, by adding the latch based comparator the accuracy of an already designed conventional two-step flash ADC can be increased. Compared with conventional two-step ADCs the comparison duration is increasing by $(2^N–1)\cdot 400$ pS, where N is the number of bits of MSB ADC, as the sampled input analog voltage firstly should be compared with comparison range separating points. For simulated configuration the area increase equals to 53.6 μm^2 (area has a strong dependence on configurable capacitance size). On the other

hand, the ADC is becoming more sensitive to its input change (4 mV offset) and can be used in designs where a high accuracy and a comparison reliability are critical, for it excludes the chance of wrong coarse conversion.

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